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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, TUAN	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,695	WAKAYAMA ET AL.	
	Examiner	Art Unit	
	TUAN A PHAM	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,10-21,23-26 and 29-41* is/are rejected.

7)☒ Claim(s) *6,8,9,22,27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/10/03,9/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 01/10/2003 and 09/03/2003 has been considered by Examiner and made of record in the application file.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 7, 10, 13-16, 23-26, 29-30, 32-37, and 38-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz").

Regarding claim 1, Tomasz teaches a method and an integrated tuner, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

a signal input on the substrate (see figure 2, RFin input, col.3, ln.1-5);

a local oscillator (LO) generation circuit, disposed on the substrate, that is configured to generate a differential local oscillator signal (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

a differential direct conversion mixer, disposed on said substrate, and coupled to said signal input and the differential LO oscillator signal (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

a differential tunable low pass filter, disposed on the substrate, and coupled to an output the differential direct conversion mixer (see figure 5, low pass filter 102, col.1, 55-65).

Regarding claim 7, Tomasz further teaches the integrated tuner comprising a LO correction circuit that is configured to adjust an amplitude level of the differential LO oscillator signal to improve performance of a differential direct conversion mixer (see figure 2, DSP 78, col.5, ln.22-56, DSP control the amplitude of the LO).

Regarding claim 10, Tomasz further teaches the integrated tuner wherein the differential direct conversion mixer included an in-phase (I) mixer and a quadrature (Q) mixer (see figure 2, mixer 68, mixer 70, col.4, ln.22-36).

Regarding claim 13, Tomasz further teaches the integrated tuner further comprising a differential low pass filter coupled between an output of the differential direct conversion mixer and an input to the differential tunable low pass filter (see figure 1, mixer 44, mixer 46, first low pass filter 48, second low pass filter 48).

Regarding claim 14, Tomasz further teaches the integrated tuner wherein a cutoff frequency of the differential low pass filter is substantially fixed and selected to remove a sum frequency that is generated by the differential direct conversion mixer (see col.4, ln.30-35).

Regarding claim 15, Tomasz further teaches the integrated tuner wherein the signal input receives a radio frequency signal having a plurality of channels (see figure 2, col.3, ln.1-5).

Regarding claims 16 and 41, Tomasz further teaches the integrated tuner wherein the plurality of channels occupies a frequency range from approximately 950 MHZ to 2150 MHz (see figure 2, col.3, ln.1-5).

Regarding claim 23, Tomasz further teaches the integrated tuner further comprising a first baseband amplifier connected between the differential direct conversion mixer and the tunable differential low pass filter, and a second baseband amplifier connected to an output of the tunable differential low pass filter (see figure 2, amplifier 92, amplifier 96, col.4, ln.22-25).

Regarding claims 24, 26 and 40, Tomasz further teaches the integrated tuner a means for detecting a DC offset voltage at an output of the second amplifier; and a means for canceling the DC offset voltage at an output of the first amplifier (see col.4, ln.36-57).

Regarding claim 25, Tomasz further teaches the integrated tuner wherein the means for canceling comprises: means for converting the DC offset voltage to a corresponding differential current; and means for combining the differential current out-of-phase with a differential current at an output of the first amplifier (see col.4, ln.36-57).

Regarding claim 29, Tomasz teaches a method and an integrated tuner, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

a signal input, disposed on the substrate, capable of receiving a RF signal having a plurality of channels (see figure 2, RFin input, col.3, ln.24-27);

a local oscillator (LO) generation circuit, disposed on the substrate, configured to generate in-phase (I) and quadrature (Q) LO signals (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

an I/Q mixer, disposed on the substrate and coupled to the signal input and the LO generation circuit, the differential I/Q mixer configured to down-convert a selected channel in the plurality of channels directly to baseband, the selected channel determined by a frequency of the I and Q LO signals (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

a first tunable lowpass filter, disposed on the substrate, and coupled to an I output of the I/Q mixer (see figure 1, low pass filter 48, col.1, ln.55-65); and

a second tunable lowpass filter, disposed on the substrate, coupled to a Q output of the I/Q mixer (see figure 5, low pass filter 48, col.1, 55-65).

Regarding claim 37, Tomasz teaches a method, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

generating a differential local oscillator signal on a common substrate (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

mixing the received RF signal with the differential local oscillator signal on the common substrate, a frequency of the local oscillator signal determined so that a selected channel of the plurality of channels is down-converted directly to baseband during the mixing step to produce a differential baseband signal (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

filtering the differential baseband signal in a differential tunable filter on the common substrate, to remove unwanted frequencies above a cutoff frequency, to produce a filtered baseband signal (see figure 5, low pass filter 102, col.1, 55-65, the low pass filter is filtering out the high frequency, which is unwanted frequency).

Regarding claims 30 and 39, Tomasz further teaches the integrated tuner a means for tuning a first cutoff frequency of the first tunable low pass filter and a second cutoff frequency of the second tunable low pass filter, the means for tuning disposed on the substrate (see col.4, ln.21-36).

Regarding claim 32, Tomasz further teaches the integrated tuner wherein the RF signal, and the I and Q LO signals are all differential signals, wherein the I/Q mixer has differential inputs and outputs, wherein the first tunable low pass filter and the second tunable low pass filter has differential inputs and outputs (see figure 1, mixer 44, mixer 48, low pass filter 48).

Regarding claims 33 and 38, Tomasz further teaches the integrated tuner a means for adjusting a frequency of the I and Q LO signals, to thereby change the selected channel that is down-converted to baseband (see figure 2, col.3, ln.17-59).

Regarding claim 34, Tomasz further teaches the integrated tuner a first variable gain amplifier (VGA) coupled between an I output of the I/Q mixer and the first tunable lowpass filter; a second variable gain amplifier (VGA) coupled between an Q output of the I/Q mixer and the second tunable low pass filter; a first buffer amplifier coupled to an output of the first VGA; and a second buffer amplifier coupled to an output of the second VGA (see figure 2, first amplifier 92, second amplifier 96, first gain amplifier 94, second gain amplifier 98, col.4, ln.21-25).

Regarding claim 35, Tomasz further teaches the integrated tuner a first DC servo circuit configured to detect a DC offset voltage at an output of the first buffer amplifier and cancel the DC offset at an output of the first VGA; and a second DC servo circuit configured to detect a DC offset voltage at an output of the second buffer amplifier and cancel the DC offset at an output of the second VGA (see figure 2, first and second DC offset circuit, col.4, ln.37-57).

Regarding claim 36, Tomasz further teaches the integrated tuner wherein the first DC servo circuit includes: means for converting the DC offset voltage at an output of the first buffer amplifier to a DC offset current; means for combining the DC offset current approximately 180 degrees out-of-phase with a current in the VGA (see figure 2, first and second DC offset circuit, col.4, ln.37-57).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz") in view of Yamawaki et al. (Pub. No.: US 2003/0143960, hereinafter, "Yamawaki").

Regarding claim 2, Tomasz teaches a method and an integrated tuner, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

a signal input, disposed on the substrate, capable of receiving a RF signal having a plurality of channels (see figure 2, RFin input, col.3, ln.1-5);

a local oscillator (LO) generation circuit, disposed on the substrate, configured to generate in-phase (I) and quadrature (Q) LO signals (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

an I/Q mixer, disposed on the substrate and coupled to the signal input and the LO generation circuit, the differential I/Q mixer configured to down-convert a selected channel in the plurality of channels directly to baseband, the selected channel determined by a frequency of the I and Q LO signals (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

a first tunable lowpass filter, disposed on the substrate, and coupled to an I output of the I/Q mixer (see figure 1, low pass filter 48, col.1, ln.55-65); and

a second tunable lowpass filter, disposed on the substrate, coupled to a Q output of the I/Q mixer (see figure 1, low pass filter 48, col.1, 55-65).

It should be noticed that Tomasz fails to teach a plurality of voltage controlled oscillators (VCOs), each of the VCOs configured to generate the differential local oscillator signal over a different frequency band. However, Yamawaki teaches such features (see figure 1, plurality VCO, col.2, [0034]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamawaki to Tamasz, in order to save space as suggested by yamawaki at column 2, [0020].

Regarding claim 3, Yamawaki further teaches the integrated tuner wherein one of the VCOs is selected to provide the differential local oscillator signal based on a desired frequency for the differential local oscillator signal (see figure 1, plurality VCO, col.2, [0034]).

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz") in view of Kung (U.S. Patent No.: 6,037,825).

Regarding claim 11, Tomasz teaches a method and an integrated tuner, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

a signal input, disposed on the substrate, capable of receiving a RF signal having a plurality of channels (see figure 2, RFin input, col.3, ln.1-5);

a local oscillator (LO) generation circuit, disposed on the substrate, configured to generate in-phase (I) and quadrature (Q) LO signals (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

an I/Q mixer, disposed on the substrate and coupled to the signal input and the LO generation circuit, the differential I/Q mixer configured to down-convert a selected

channel in the plurality of channels directly to baseband, the selected channel determined by a frequency of the I and Q LO signals (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

a first tunable lowpass filter, disposed on the substrate, and coupled to an I output of the I/Q mixer (see figure 1, low pass filter 48, col.1, ln.55-65); and

a second tunable lowpass filter, disposed on the substrate, coupled to a Q output of the I/Q mixer (see figure 1, low pass filter 48, col.1, 55-65).

It should be noticed that Tomasz fails to teach the differential direct conversion mixer includes: an RF transconductance circuit that is configured to convert a differential signal received at the signal input to a differential current; and a LO switching circuit configured to switch the differential signal between outputs of the differential direct conversion mixer at a rate determined by the differential LO signal. However, Kung teaches such features (see figure 1, I1, I2, col.3, ln.39-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kung to Tamasz, in order to reduce the DC bias in the mixer as suggested by Kung at column 1, lines 39-54.

Regarding claim 12, Kung further teaches the integrated tuner the RF transconductance circuit includes a pair of field effect transistors to convert the differential signal to the differential current, the differential direct conversion mixer further comprising a means for adding DC current to the pair of transistors to minimize flicker noise (see figure 2, col.4, ln.30-52).

8. Claims 17-8, 21, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz") in view of Okanobu et al. (U.S. Patent No.: 5,757,921, hereinafter, "Okanobu").

Regarding claims 17 and 31, Tomasz teaches a method and an integrated tuner, comprising (see figure 5):

a substrate (see figure 5, tuner unit, col.6, ln.52-56, tuner is an integrated circuit that should be included a substrate);

a signal input, disposed on the substrate, capable of receiving a RF signal having a plurality of channels (see figure 2, RFin input, col.3, ln.1-5);

a local oscillator (LO) generation circuit, disposed on the substrate, configured to generate in-phase (I) and quadrature (Q) LO signals (see figure 2, local oscillator, col.3, ln.45-55, col.4, ln.37-57);

an I/Q mixer, disposed on the substrate and coupled to the signal input and the LO generation circuit, the differential I/Q mixer configured to down-convert a selected channel in the plurality of channels directly to baseband, the selected channel determined by a frequency of the I and Q LO signals (see figure 2, RFin input, mixer 68, mixer 70, baseband processor 78, col.4, 22-36);

a first tunable lowpass filter, disposed on the substrate, and coupled to an I output of the I/Q mixer (see figure 1, low pass filter 48, col.1, ln.55-65); and

a second tunable lowpass filter, disposed on the substrate, coupled to a Q output of the I/Q mixer (see figure 1, low pass filter 48, col.1, 55-65).

It should be noticed that Tomasz fails to teach the low pass filter includes a plurality of integrators, each integrator having a resistor and a capacitor, wherein a cutoff frequency of the low pass filter is tuned by adjusting at least one of the resistor or the capacitor in the integrators.. However, Okanobu teaches such features (see figure 6, LPF 70, variable resistor R72, col.9, ln.44-67, col.10, ln.1-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Okanobu to Tamasz, in order to select a particular frequency.

Regarding claim 18, Okanobu further teaches the integrated tuner the capacitor is fixed and the cutoff frequency is tuned by adjusting a value of the resistor (see figure 6, LPF 70, variable resistor R72, col.9, ln.44-67, col.10, ln.1-20).

Regarding claim 21, Okanobu further teaches the integrated tuner the capacitor is a metal oxide semiconductor capacitor (MOSCAP) (the low pass filter is an integrated in one chip, therefore, the capacitor should be a MOSCAP for transmit a high frequency).

9. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz") in view of Yamawaki et al. (Pub. No.: US 2003/0143960, hereinafter, "Yamawaki") as applied to claim 1 above, and further in view of Okanobu (U.S. Patent No.: 6,529,100).

Regarding claim 4, Tomasz and Yamawaki, in combination, fails to teach the LO generation circuit further comprises a plurality of polyphase circuits that correspond to the plurality of VCOs, each polyphase circuit configured to generate in-phase (I) and quadrature (Q) differential local oscillator signals based on an output of a corresponding VCO. However, Okanobu teaches such features (see figure 1, figure 2, polyphase filter 17, col.7, ln.1-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Okanobu to Tomasz and Yamawaki, in order to process the IF signal.

Regarding claim 5, Okanobu further teaches the integrated tuner the VCOs are connected to the plurality of the polyphase circuits by a plurality of amplifiers, wherein a VCO is selected by enabling one or more of the amplifiers that correspond to the selected VCO, and disabling more one or more amplifiers that do not correspond to the selected VCO (see col.7, ln.1-37).

10. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz et al. (U.S. Patent No.: 6,031,878, hereinafter, "Tomasz") in view of Okanobu et al. (U.S. Patent No.: 5,757,921, hereinafter, "Okanobu") as applied to claim 1 above, and further in view of Koike (U.S. Patent No.: 6,246,864).

Regarding claim 19, Tomasz and Okanobu, in combination, fails to teach the resistor is a bank of parallel resistors having corresponding series-connected switches, so that the cutoff frequency is tuned by controlling the series-connected switches. However, Koike teaches such features (see figure 2, resistor VR1-VRn, switch, col.7, ln.40-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Okanobu to Tomasz and Yamawaki, in order to select a particular frequency band.

Regarding claim 20, Okanobu further teaches the integrated tuner the bank of parallel resistors have corresponding values that are binarily weighted relative to each other, and thereby the cutoff frequency is adjustable in fixed increments (see figure 2, resistor VR1-VRn, switch, col.7, ln.40-50).

Allowable Subject Matter

11. Claims 6, 8-9, 22, and 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In order to expedite the prosecution of this application, the applicants are also requested to consider the following references. Although Lindstrom et al. (US patent No.: 6,731,712), Prentice (Pub. No. US 2002/0042255), and Wang (U.S. Patent No. 6,160,571) are not applied into this Office Action; they are also called to Applicants attention. They may be used in future Office Action(s). These references are also concerned for supporting the system and method for detecting and correcting phase error between differential signals.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tuan A. Pham** whose telephone number is (703) 305-4987. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Curtis Kuntz can be reached on (703) 305-4708 and

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Art Unit 2643
March 11, 2005
Examiner

Tuan Pham

BINH TIEU
PRIMARY EXAMINER